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1 [Performance measurements for multithreaded programs](#)



Minwen Ji, Edward W. Felten, Kai Li

 June 1998 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1998 ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems SIGMETRICS '98/PERFORMANCE '98,**
 Volume 26 Issue 1

Publisher: ACM Press

 Full text available: [pdf\(1.37 MB\)](#)

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Multithreaded programming is an effective way to exploit concurrency, but it is difficult to debug and tune a highly threaded program. This paper describes a performance tool called Tmon for monitoring, analyzing and tuning the performance of multithreaded programs. The performance tool has two novel features: it uses "thread waiting time" as a measure and constructs thread waiting graphs to show thread dependencies and thus performance bottlenecks, and it identifies "semi-busy-waiting" points w ...

2 [Eraser: a dynamic data race detector for multithreaded programs](#)



Stefan Savage, Michael Burrows, Greg Nelson, Patrick Sobalvarro, Thomas Anderson

 November 1997 **ACM Transactions on Computer Systems (TOCS),** Volume 15 Issue 4

Publisher: ACM Press

 Full text available: [pdf\(136.04 KB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Multithreaded programming is difficult and error prone. It is easy to make a mistake in synchronization that produces a data race, yet it can be extremely hard to locate this mistake during debugging. This article describes a new tool, called Eraser, for dynamically detecting data races in lock-based multithreaded programs. Eraser uses binary rewriting techniques to monitor every shared-memory reference and verify that consistent locking behavior is observed. We present several case studies ...

Keywords: binary code modification, multithreaded programming, race detection

3 [Calibrating the simulation model of the IBM system/360 time sharing system](#)

P. E. Barker, H. K. Watson

 December 1969 **Proceedings of the third conference on Applications of simulation**

Publisher: Winter Simulation Conference

 Full text available: [pdf\(597.29 KB\)](#)

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A GPSS/360 model was developed to support the IBM System/360 Time Sharing System


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1 [From trace generation to visualization: a performance framework for distributed parallel systems](#)

C. Eric Wu, Anthony Bolmarcich, Marc Snir, David Wootton, Farid Parpia, Anthony Chan, Ewing Lusk, William Gropp

November 2000 **Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)****Publisher:** IEEE Computer SocietyFull text available: [pdf\(544.42 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)[Publisher Site](#)

In this paper we describe a trace analysis framework, from trace generation to visualization. It includes a unified tracing facility on IBM SP systems, a self-defining interval file format, an API for framework extensions, utilities for merging and statistics generation, and a visualization tool with preview and multiple time-space diagrams. The trace environment is extremely scalable, and combines MPI events with system activities in the same set of trace files, one for each SMP node. Sin ...

Keywords: distributed parallel systems, SMP clusters, trace generation, intervalfile format, multiple time-space diagrams, trace visualization

2 [Mixed mode execution with context threading](#)

Mathew Zaleski, Marc Berndt, Angela Demke Brown

October 2005 **Proceedings of the 2005 conference of the Centre for Advanced Studies on Collaborative research CASCON '05****Publisher:** IBM PressFull text available: [pdf\(162.98 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Interpreters are widely used to implement portable language runtime environments. Programs written in these languages may benefit from performance beyond that obtainable by optimizing interpretation alone. A modern high-performance mixed-mode virtual machine (VM) includes a method-based Just In Time (JIT) compiler. A method-based JIT, however, requires the up-front development of a complex compilation infrastructure before any performance benefits are realized. Ideally, the architecture for a mixe ...

3 [Impact of sharing-based thread placement on multithreaded architectures](#)



R. Thekkath, S. J. Eggers

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2


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1 [Regular contributions: A trace-level value predictor for Contrail processors](#)



Takenori Koushiro, Toshinori Sato, Itsujiro Arita

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Publisher: ACM Press

Full text available: [pdf\(490.59 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

Contrail processors utilize multithreading for improving energy efficiency. In Contrail, an execution of an application is divided into two streams. One is called the speculation stream. It consists of the main part of the execution and is dispatched into the fast functional units. However, several regions of the execution are skipped by utilizing trace-level value prediction. The other stream is called the verification stream. It supports the speculation stream by verifying each data prediction ...

Keywords: chip multi processors, energy efficiency, simultaneous multithreading, traceconstruction, value prediction

2 [Control independence in trace processors](#)

Eric Rotenberg, Jim Smith

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: [pdf\(1.40 MB\)](#) [Publisher Site](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Branch mispredictions are a major obstacle to exploiting instruction-level parallelism, at least in part because all instructions after a mispredicted branch are squashed. However, instructions that are control independent of the branch must be fetched regardless of the branch outcome, and do not necessarily have to be squashed and re-executed. Control independence exists when the two paths following a branch re-converge. A trace process ...

3 [SPAA revue: The potential in energy efficiency of a speculative chip-multiprocessor](#)



Yuu Tanaka, Toshinori Sato, Takenori Koushiro

June 2004 **Proceedings of the sixteenth annual ACM symposium on Parallelism in algorithms and architectures**

Publisher: ACM Press

Full text available: [pdf\(146.44 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

While lower supply voltage is effective for energy reduction, it suffers performance loss. To mitigate the loss, we propose to execute only the part, which does not have any



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IEEE CNF IEEE Conference Proceeding

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